REMARKS

Claims 1-32 are pending in the present application.

Claims 1-5, 14, 17-21, and 30 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Dieffenderfer et al. (U.S. Patent Publication Number 2004/0186964) (hereinafter "Dieffenderfer") in view of Steiss et al. (U.S. Patent Number 6,895,493) (hereinafter "Steiss"). Applicant respectfully traverses this rejection and requests reconsideration in view of the following remarks.

Claims 6-13, 15, 16, 22-29, 31, and 32 are objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant has not, at this juncture, rewritten the claims into independent form since Applicant believes the independent claims to patentably distinguish over the cited reference as described below.

Applicant's claim 1 recites a mechanism for filtering snoop requests to a cache memory comprising in pertinent part

> "a cache controller configured to receive a transaction request including an address and to generate an index for accessing said storage by performing a hash function on said address;
>
> wherein, said cache controller is further configured to selectively generate a snoop operation to said cache memory for said transaction request dependent upon **a snoop filter indication** stored in said storage **that corresponds to said address**."

The Examiner asserts the combination of Dieffenderfer and Steiss teach the limitations recited in Applicant's claim 1. Applicant respectfully disagrees with the examiner's characterizations of both Dieffenderfer and Steiss and the alleged motivation to combine the references. Furthermore, Applicant submits the combination does not produce the Applicant's invention as suggested by the Examiner.

More particularly, Dieffenderfer discloses at paragraph [0021]

> "[0021] In order to accomplish this snoop filtering, the non-originating master 10b must have knowledge of whether it could share the requested data with the originating master 10a. There are a variety of techniques and/or snoop filtering device by which the non-originating master 10b could determine whether it could potentially share the requested data with the originating master 10a. One such technique involves a program resident in each master 10a. . . 10n which "knows" what tasks each master 10a. . . 10n is performing and has performed. This can be a simple as "knowing" that certain masters 10a. . . 10n would not have data in the requested address range; or it could be more complex. From this information, the non-originating master 10b can know that it does not need to snoop its resources for the data requested by master 10a. The knowledge may be represented in different ways. One mechanism or device is a simple one bit flag in a register contained within non-originating master 10b for each originating master 10a. . . 10n, wherein a "1" indicates that that specific master 10 could possibly share data with master 10b, and a "0" indicates this specific master 10 could not possibly share data with 10a. . . 10n. When the non-originating master 10b receives the snoop request from bus 14 it will also receive a signal indicating which master 10a. . . 10n originated the request. Master 10b then checks the flag associated with master 10a to see if it could be sharing the requested data with master 10a. If master 10b determines in step 45 that it cannot be sharing the requested data with master 10a it will not check its resources for the requested data and will immediately respond to bus 14 indicating that it does not have the requested data as shown in step 52. If master 10b determines that it could be sharing the requested data with master 10a in step 45, then master 10b will check all of its resources for the requested data as shown in step 46 and respond to bus 14 indicating the results of the snoop as shown in step 52. From this point on, the operation of the snooping is similar to the above referenced application as dictated by the particular protocol." (Emphasis added)

From the foregoing, Applicant submits Dieffenderfer is teaching using a 1-bit flag in a register that corresponds to a specific master. Each flag bit represents an indication whether a corresponding master can share the data in the non-originating master's cache. This is clearly different than "**a snoop filter indication** stored in said storage **that corresponds to said address**."

Dieffenderfer also discloses at paragraph [0024] "Address: This is the **address of the snoop request**. This could be used by the non-originating snooper to filter the

snoop." (Emphasis added) However, Dieffenderfer is silent as to how the address of the snoop request may be used. Applicant submits any inference that Dieffenderfer suggests using the address to do anything specific is merely speculation using the benefit of hindsight provided by Applicant's invention.

Thus, Dieffenderfer does not teach using the address to access the register, much less the hash of the address, particularly since the register is associated with a respective master, and not a cache line address. Accordingly, Applicant submits Dieffenderfer **does not teach or disclose** "a cache controller configured to receive a transaction request including an address and to generate an index for accessing said storage by performing a hash function on said address" or "wherein, said cache controller is further configured to selectively generate a snoop operation to said cache memory for said transaction request dependent upon a **snoop filter indication** stored in said storage **that corresponds to said address**" as recited in Applicant's claim 1.

The Examiner acknowledges Dieffenderfer does not teach "using a hash function on the address to generate an index, which is then use to determine if the cache should be snooped." However, the Examiner asserts Steiss teaches the limitation. Applicant respectfully disagrees. Specifically, Steiss discloses at col. 1, line 51 through col. 2, line 2

> "According to one embodiment of the present invention, there is provided a system for processing data that includes storing **a write operation** in a store buffer. The write operation indicates that a first data element is to be written to a memory array element. The write operation includes a first address associated with a location in the memory array element to where the first data element is to be written. A read operation may also be received at the store buffer. The read operation indicates that a second data element is to be read from the memory array element. The read operation includes a second address associated with a location in the memory array element from where the second data element is to be read. **A hashing operation is executed on the first and second addresses** at any suitable time interval **such that a first hashed address and a second hashed address are respectively produced. The first and second hashed addresses are compared such that if they match each other the first data element is written to the memory array** element before the read operation is executed for the second data element."

From the foregoing, Applicant submits Steiss is teaching using a hash function on two addresses associated with respective write and read operations for the purpose of comparing the resultant hashed value to determine if they are the same. Thus, Applicant submits Steiss is not using the hash function on transaction request address to generate an index for accessing a storage.

Although Dieffenderfer discloses a way to implement cache snoop filtering, Applicant submits Dieffenderfer does it in a different way. Applicant submits that key aspects of Applicant's claimed invention are not taught or suggested by Dieffenderfer, as described above. Specifically, Dieffenderfer does not teach using any indexing to access his registers. Dieffenderfer teaches that the registers correspond to respective master devices and not cache line addresses. Dieffenderfer is silent as to how a snoop address may be used. In addition, Steiss is only teaching hashing of a write address and a read address to enhance the speed at which the hash results of the two addresses are able to be compared. Thus Applicant submits, combining Steiss with Dieffenderfer would NOT produce Applicant's claimed invention. Furthermore, based on the above discussion, Applicant submits a person of ordinary skill in the art would not be motivated to combine these references.

Accordingly, Applicant submits neither Dieffenderfer nor Steiss, taken either singly or in combination, teach or suggest the combination of features recited in Applicant's claim 1. Thus, Applicant submits claim 1, along with its dependent claims, patentably distinguishes over Dieffenderfer in view of Steiss for the reasons given above.

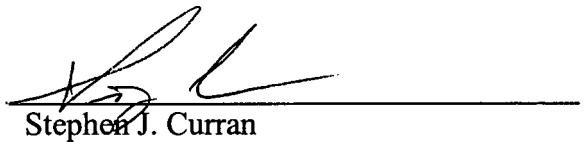
Applicant's claim 17 recites features similar to the features recited in claim 1. Accordingly, Applicant submits claim 17, along with its dependent claims, patentably distinguishes over Dieffenderfer in view of Steiss for at least the reasons given above.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5181-95901/SJC.

Respectfully submitted,



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